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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,522	02/06/2004	Herb H. Huang	021653-000900US	6545

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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 01/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/773,522	HUANG ET AL.
	Examiner	Art Unit
	N. Drew Richards	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2005 and 24 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The replacement drawings were received on 7/8/05. These drawings are acceptable.

Claim Objections

3. Claim 1 is objected to because of the following informalities: claim 1 line 14 should recite "from **said** trench isolation region" as the trench isolation region has been previously recited; claim 1 line 15 should recite "**said** source drain regions" as the source drain regions have previously been recited.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4 and 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu (US 2005/0006694 A1) in view of Shiau (US Patent No. 6,372,580 B1).

Liu teach a method for manufacturing ROM memory devices, the method comprising:

- forming a trench isolation structure 150 within a cell region of a semiconductor substrate 110, the cell region being an array region for ROM memory devices (figures 6A-6C show the steps for forming the trench isolation 150; as seen in figures 3A and 3C the trench isolation 150 is within a cell region which is part of an array region for ROM devices, figure 3A shows a 3x3 array), the trench isolation structure being provided to separate a bit line region of the cell from another bit line region from another cell (as seen in figure 3A the trench isolation structure 150 isolates the bit line regions 120 between the gate structures 124); and
- forming a gate structure 124 within the cell region (figures 3A and 3B).

Liu further teaches buried bit lines 120 in the cell regions and source/drain regions 120 (figures 3A and 3B, it is noted that the buried bit lines 120 also function as the source/drain regions 120 such that a separate structure is not needed for the bit line and source/drain regions). Liu fails to explicitly teach the steps of forming a sidewall spacer on the gate structure as claimed, applying a refractory metal layer as claimed, alloying the refractory metal layer to the gate structure and exposed portions of source/drain regions to form silicide regions as claimed, or selectively removing the refractory metal layer as claimed.

Shiau teach a method of manufacturing ROM memory devices including an array of buried bit lines BN^+ and polysilicon word lines POLY (gate structures) similar to that

of Liu but also including salicide regions. Specifically, Shiau teach forming a first sidewall spacer 47 overlying a first side of the gate structure POLY and a second sidewall spacer 47 overlying a second side of the gate structure POLY (figures 10B and 10D, column 4 lines 47-48), applying a refractory metal overlying the entire substrate including the gate structure POLY (word lines) including the first and second sidewall spacers 47 (column 4 line 56 through column 5 line 4), heat treating to form silicide regions 51 overlying the gate structure POLY and exposed portions of the source/drain regions BN^+, and selectively removing the refractory metal layer from the sidewall spacers and isolation regions (figures 11A-11D and column 4 line 56 through column 5 line 4). It is noted that Shiau does not explicitly state their heat treatment resulting in "alloying" the refractory metal. Nonetheless, this is implicitly taught by Shiau as alloying is inherent in heat treating to form the silicide. That is, the silicon and the metal inherently alloy together in forming the silicide.

Liu and Shiau are from the same field of endeavor. At the time of the invention, it would have been obvious to one of ordinary skill in the art to employ the salicide process of Shiau in the ROM fabrication method of Liu. The motivation for doing so is to improve operational speed of the memory cells by adding the silicide layer to reduce the word line and buried bit line resistance (Shiau abstract). Therefore, it would have been obvious to combine Liu with Shiau to obtain the invention of claim 1.

In combining the salicide process of Shiau into the ROM fabrication method of Liu, the first and second sidewall spacer structures would necessarily be configured to overlap a portion of the trench isolation structure 150 and extend over and overlap a

portion of the source drain regions since the gate structure 124 overlies the trench isolation structure 150 and the source drain regions are formed below the side surface of the gate. In providing the sidewall spacers using the method taught by Shiau (column 4 lines 47-54) the sidewall spacers would be formed along the entire length of the gate structure. It is noted that this sidewall spacers configuration is the same as in the instant application (as shown in figures 2-4 of the instant application) and thus is considered to be configured to separate the gate structure from the trench isolation region and to separate the gate structure from the source drain regions.

Further, in the combination the refractory metal layer of Shiau would be applied to the gate structure 124 including sidewall spacers and exposed portions of the trench isolation structure 150 since the refractory metal is deposited over the entire substrate surface.

With regard to claim 2, the refractory metal layer of Shiau is titanium or cobalt (column 4 line 56).

With regard to claim 3, the trench isolation region of Liu is an STI region (paragraph 35).

With regard to claim 4, the STI region comprises silicon dioxide (paragraph 36).

With regard to claim 6, the first and second sidewall spacers of Shiau are a dielectric material (column 4 line 52).

With regard to claim 7, the buried bit line structure of Liu is within the source/drain region.

With regard to claim 8, the trench isolation 150 is within the substrate at a predetermined depth which is greater than a junction depth of the buried bit line 120 (figure 3C).

6. Claims 5 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu with Shiau as applied to claims 1-4 and 6-8 above, and further in view of Iwata et al. (US 2004/0262650 A1).

Liu with Shiau do not explicitly disclose a channel region using a length of about 0.25 micron and less or the gate structure having a width of 0.25 micron and less. Iwata et al. teach semiconductor devices. Iwata et al. teach in paragraph 3 that recently the integration level of semiconductor devices is becoming higher and higher and thus there is a demand for smaller elements. Iwata et al. teach in paragraph 24 that the gate electrode (gate structure) is formed to a width of 100 nm (0.1 micron). It is noted that this paragraph relates to figure 44, which shows that channel length as the same as the gate width, thus Iwata teach both the gate structure and channel length of less than 0.25 micron.

Liu with Shiau and Iwata et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to one of ordinary skill in the art to form the gate structure width and channel length to 0.25 micron or less. The motivation for doing so is to meet the demand for smaller elements for higher integration. Therefore, it would have been obvious to combine Liu and Shiau with Iwata et al. to obtain the invention of claims 5 and 9.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liu with Shaiu as applied to claims 1-4 and 6-8 above, and further in view of Chang (US Patent No. 5,506,160).

Liu and Shaiu each teach an array of ROM cells (see figure 3A of Liu and figure 4 of Shiau, for example) but do not explicitly disclose their array having at least eight cells by eight cells. Nonetheless, it is considered obvious to form a ROM array to have at least eight cells by eight cells. Each cell represents one bit of data. Chang teach a ROM array in figure 5, for example. Chang et al. teach forming the array to be a 64 Mbit array. As one of ordinary skill in the art would recognize, a 64 Mbit array has at least eight cells by eight cells. At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the array of Liu with Shiau to have at least eight cells by eight cells. The motivation for doing so is to meet an industry need of higher integration and larger memory arrays and to provide a greater amount of memory needed for modern electronics devices. Thus, it would have been obvious to form the array to at least eight cells by eight cells as claimed.

Response to Arguments

8. Applicant's arguments filed 7/8/05 have been fully considered but they are not persuasive.

Applicant has argued that the sidewall structures of Shiau do not extend over and overlap a portion of the silicide on the source/drain regions. This is not persuasive as

the claims as written do not require the sidewall spacer structures to overlap the silicide regions.

Applicant has also argued that the sidewall spacers of Shiau do not extend over and overlap a portion of the trench isolation structure. This is not persuasive as in the combination of Lui and Shiau, the sidewall spacers will extend over and overlap a portion of the trench isolation structure. As seen in figure 3A of Liu, the isolation structures 150 are directly aligned under the sidewalls of the gate 124), thus in adding a sidewall spacer as taught by Shiau along the sidewalls of the gate, the sidewall spacers will necessarily extend over and overlap the isolation structures.

Conclusion

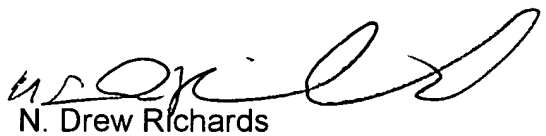
9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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